

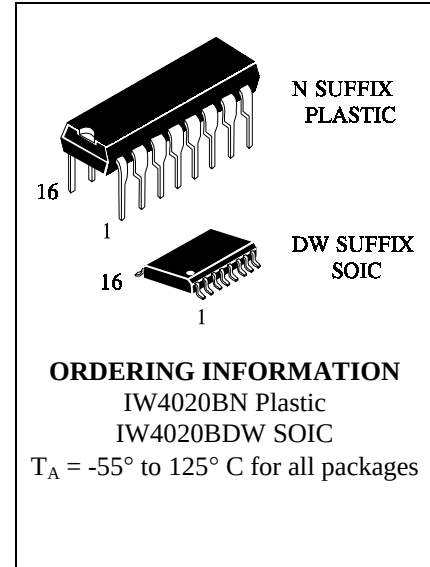
IW4020B

14 Stage Ripple-Carry Binary Counter/Divider

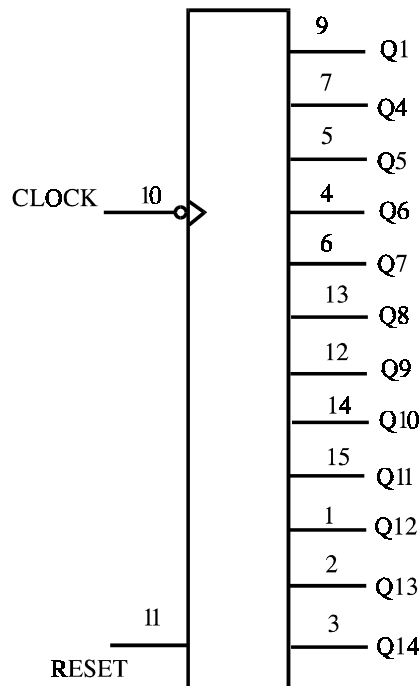
High-Voltage Silicon-Gate CMOS

The IW4020B is ripple-carry binary counter. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply



LOGIC DIAGRAM



PIN 16 = V_{CC}
 PIN 8 = GND

PIN ASSIGNMENT

Q12	1	16	V_{CC}
Q13	2	15	Q11
Q14	3	14	Q10
Q6	4	13	Q8
Q5	5	12	Q9
Q7	6	11	RESET
Q4	7	10	CLOCK
GND	8	9	Q1

FUNCTION TABLE

Inputs		Output
Clock	Reset	Output state
	L	No change
	L	Advance to next state
X	H	All Outputs are low

X=don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).
Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5V or V _{CC} - 0.5V V _{OUT} =1.0V or V _{CC} - 1.0V V _{OUT} =1.5V or V _{CC} - 1.5V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V _{IL}	Maximum Low -Level Input Voltage	V _{OUT} =0.5V or V _{CC} - 0.5V V _{OUT} =1.0V or V _{CC} - 1.0V V _{OUT} =1.5V or V _{CC} - 1.5V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0 10 15 20	5 10 20 100	5 10 20 100	150 300 600 3000	μA
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0 10 15	0.64 1.6 4.2	0.51 1.3 3.4	0.36 0.9 2.4	mA
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0 5.0 10 15	-2.0 -0.64 -1.6 -4.2	-1.6 -0.51 -1.3 -3.4	-1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
$f_{\max}$	Maximum Clock Frequency(Figure 1)	5.0 10 15	3.5 8 12	3.5 8 12	1.75 4 6	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q1 (Figure 1)	5.0 10 15	360 160 130	360 160 130	720 320 260	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Q_n to Q_{n+1} (Figure 3)	5.0 10 15	330 80 60	330 80 60	660 160 120	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figure 2)	5.0 10 15	280 120 100	280 120 100	560 240 200	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	140 60 40	140 60 40	280 120 80	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	5.0 10 15	200 80 60	200 80 60	400 160 120	ns
t_{rem}	Minimum Removal Time, Reset(Figure 2)	5.0 10 15	350 150 100	350 150 100	700 300 200	ns
t_r , t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	5.0 10 15	Unlimited			μs

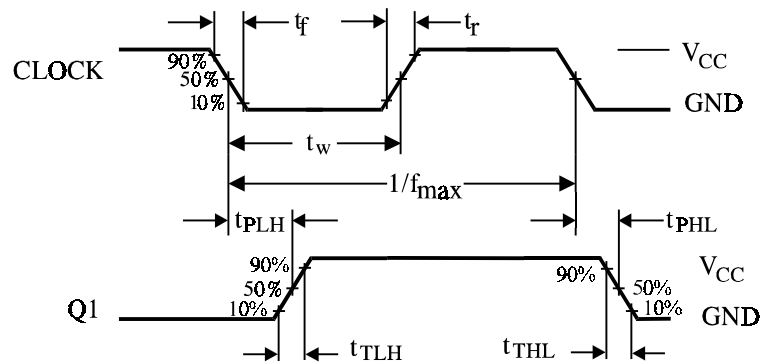


Figure 1. Switching Waveforms

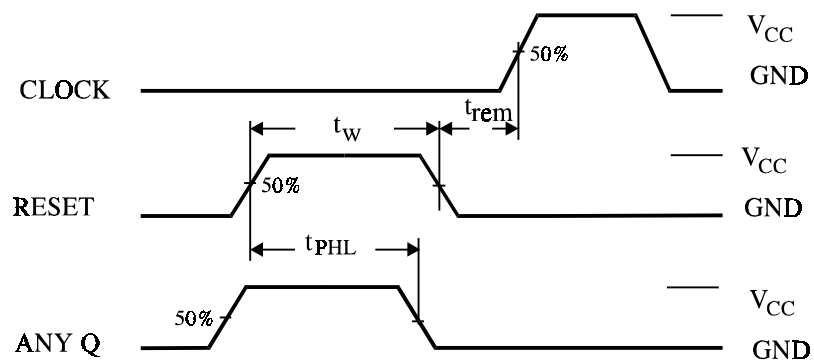


Figure 2. Switching Waveforms

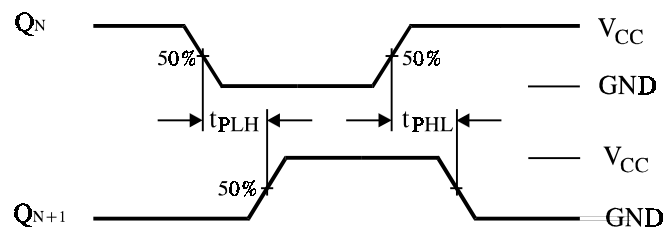
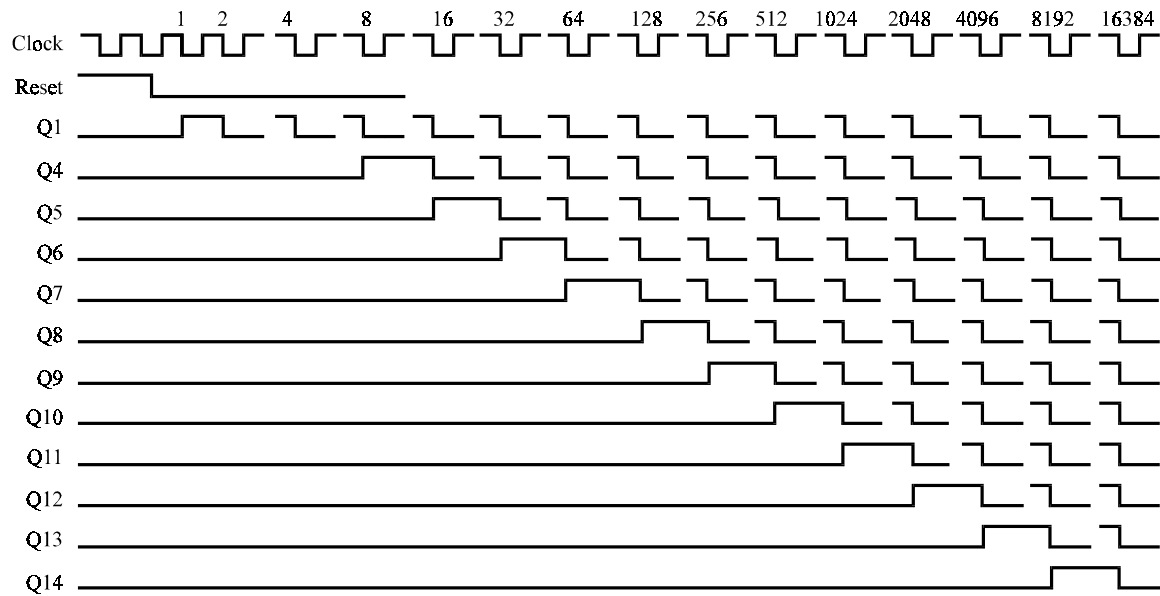
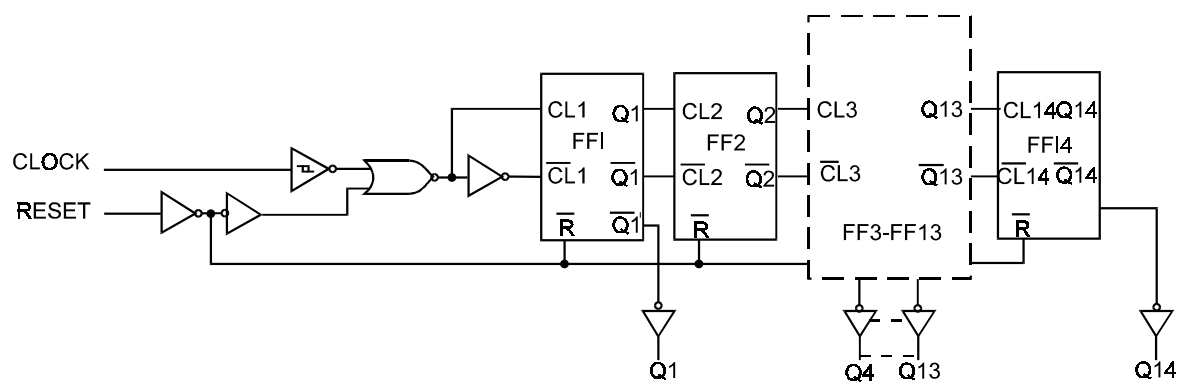


Figure 3. Switching Waveforms

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM



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